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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,465	01/27/2004	Ling Ma	IR-2444 CIP (2-3869)	3194

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EXAMINER	
KIM, SU C	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,465	MA ET AL.	
	Examiner	Art Unit	
	Su C. Kim	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's arguments with respect to claims 1, 4-10 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

The drawings were received on 2/28/2006. These drawings are acceptable.

Claim Objections

1. Claim 1 is objected to because of the following informalities: " - - less than 0.5 microns wide - -" fails to suggest unit of trench size. The examiner suggests to change "- - microns - -" to micrometer. "A termination trench formed- -" has insufficient antecedent basis for this limitation in the claim. The examiner suggests to change "A - - " to the

2. Claims 4-6 are objected to because of the following informalities;

"A semiconductor device - -" in line 1 has insufficient antecedent basis for this limitation in the claims. The examiner suggests to change "A - -" to the

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 7, & 8 are rejected under 35 U.S.C. 103(a) as being anticipated by Williams (US 2002/0019099) in view of Zeng (US Pub 2003/0205758).

Pertaining claim 1, Williams discloses all the limitation include

a synchronous semiconductor device(MOSFET is synchronous semiconductor); and

a control semiconductor device (Please note Power MOSFET is synchronous semiconductor and control semiconductor device) ;

wherein at least one of said semiconductor devices includes:

a semiconductor body of a first conductivity **(Fig. 23, 267,N-type)** which includes a channel region **(Fig. 23, 263)** of a second conductivity ((**Fig. 23, 706)** and a major surface;

an active region **(Fig. 23, 263)**formed in said semiconductor body, said active region including a trench **(Fig. 23, 261)** less than 0.5 microns wide **(paragraph 0129, trench gate is 0.5 micrometer)** extending through said channel region and a gate structure **(Fig. 23, 260, insulated 261 gate electrode structure)** disposed in said trench which includes a gate oxide layer **(Fig. 23, 261)** disposed at least on said sidewalls of said trench **(Fig. 23, oxide 275 insulated gate structure)** and a gate electrode **(Fig. 23, 293)** disposed adjacent said a gate oxide layer**(Fig. 23, 275)**: and

a termination structure**(Fig. 23, 250)**, said termination structure including, a termination trench formed in said semiconductor body, and a field oxide layer formed in said termination trench below said major surface **(Fig 12)**,

However, Williams fails to teach a field oxide layer formed in said termination trench below said major surface is thicker than said gate oxide layer.

Zeng discloses a field oxide layer formed in said termination trench below said major surface **(Fig. 15 please note the element 340 (Oxide layer) is thicker than the gate oxide layer 40).**

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention is made to provide Williams with a field oxide layer formed in said termination trench below said major surface taught by Zeng in order to produce "efficiently device" **(column 1 paragraph [0002] lines 8-10).**

Pertaining claim 7 as applied to claim 1 above, Williams discloses all the limitation includes the depth of said trench has been selected to achieve an optimum figure of merit (Williams defines the depth of trench to achieve an optimum figure of merit due to modification from previous invention).

Pertaining claim 8 as applied to claim 1 above, Williams discloses all the limitations including, trench is a stripe **(Fig. 4A).**

5. Claims 4- 6 are rejected under 35 U.S.C. 103(a) as being anticipated by Williams (US 2002/0019099) in view of Zeng (US Pub 2003/0205758) and further in view of Aoki et al. (US Pub 2002/0167046).

Pertaining claim 4 as applied to claim 1 above paragraph 4, Williams and Zeng discloses all the limitations. However, Williams and Zeng in combination fails to teach trench including an oxide mass formed at its bottom said oxide mass being thicker than said gate oxide layer. Aoki discloses trench including an oxide mass formed at its bottom said oxide mass being thicker than said gate oxide layer **(Paragraph [0045] element 7e).**

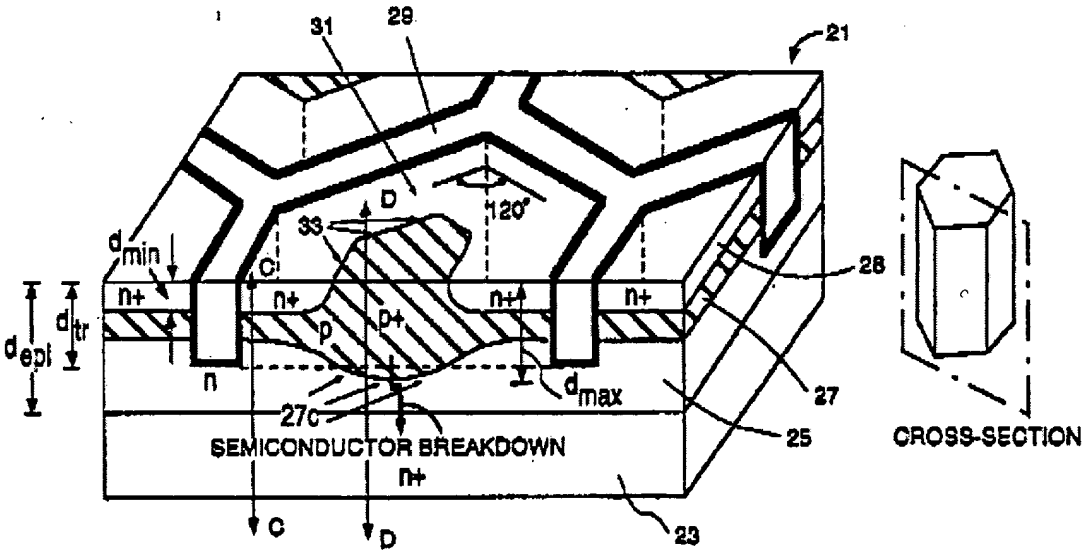
Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention is made to provide Williams and Zeng in combination with trench including an oxide mass formed at its bottom said oxide mass being thicker than said gate oxide layer taught by Aoki in order to produce "lower withstand voltage" **(paragraph [0005])**

Pertaining claim 5 as applied to claim 4 above, Williams and Zeng in combination discloses all the limitations includes semiconductor body includes conductive regions of said first conductivity **(Fig. 23, 267, N-type)** formed adjacent said trench **(Fig. 23, 261)** in said channel region **(Fig. 23, 263)**, and further comprising a semiconductor substrate of said conductivity **300**, said semiconductor body **(Fig 23, 265,267 are formed above substrate 300)** being formed over said semiconductor substrate **(300)**, wherein said

conductive regions are electrically connectable to said semiconductor substrate through invertible channels adjacent said trench **(Fig. 23, Please note the power MOSFET has conductive regions 267, which are electrically connectable to semiconductor substrate through invertible channels).**

Pertaining claim 6 as applied to claim 5 above, Williams and Zeng in combination discloses all the limitations includes conductive regions are source regions **(Fig. 24N, 302).**

6. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being anticipated by Williams (US 2002/0019099) in view of Zeng (US Pub 2003/0205758) and further in view of Bulucea et al. (US 5298442)



Bulucea discloses a semiconductor device as claimed. **See all the FIGS** where Bulucea teaches the following limitations

Pertaining claim 9 as applied to claim 1 above paragraph 4, Williams and Zeng discloses all the limitations. However, Williams and Zeng in combination fails to teach a semiconductor device including trench is a cell. Bulucea discloses a semiconductor device includes trench is a cell **(Fig. 8).**

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention is made to provide Williams and Zeng in combination with semiconductor device includes trench is a cell taught by Bulucea in order to produce "maximizes the gate dielectric breakdown voltage and also provides position of voltage breakdown initiation to allow use of controlled bulk semiconductor breakdown. " **(Column 1 lines 59-61)**

Pertaining claim 10 as applied to claim 9 above, Williams and Zeng discloses all the limitations. However, Williams and Zeng in combination fails to teach a semiconductor device includes cell is hexagonal. Bulucea discloses the cell is hexagonal. **(Fig. 8)**

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Su C. Kim whose telephone number is (571) 272-5972. The examiner can normally be reached on Monday - Thursday, 9:00AM to 7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5/12/2006
Su C. Kim

Brook Kebede

BROOK KEBEDE
PRIMARY EXAMINER